**Laboratory Report Cover Sheet**

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

**Name :**

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment:**

**Date of Conduction:**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

**11. Design of sequential circuits SR Flip-Flop and D Latch**

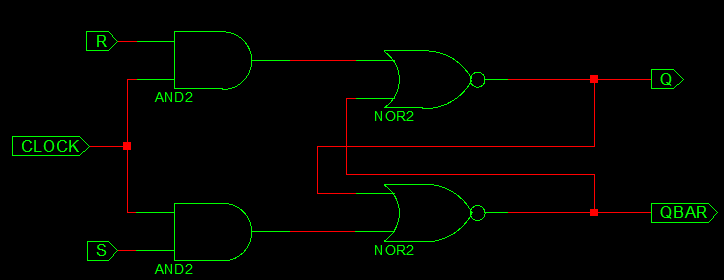
**Aim:** To design and implement a sequential circuit SR flip-flop and D latch.

**Software Required:**

Xilinx ise & ModelSim

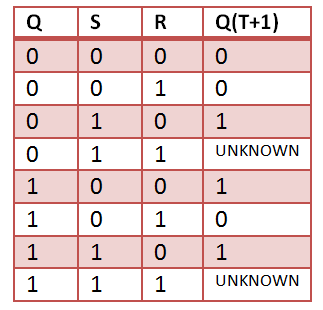
#### Theory:

A flip-flop circuit can be constructed from two NAND gates or two NOR gates. These flip-flops are shown in Figure 1. Each flip-flop has two outputs, Q and Q’, and two inputs, set and reset. This type of flip-flop is referred to as an SR flip-flop.

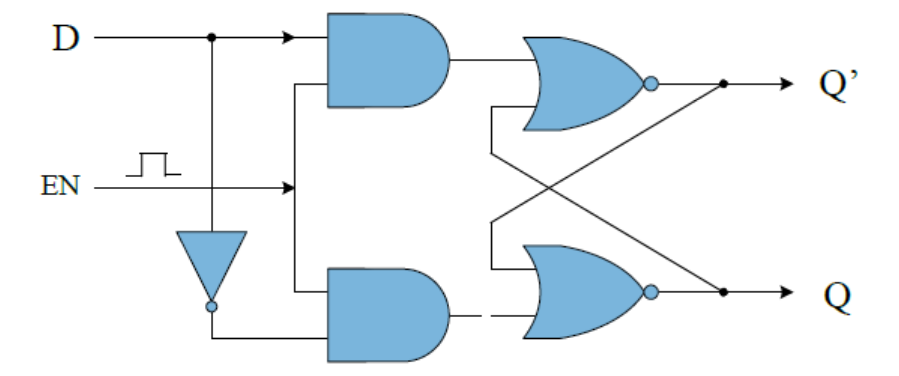


**Fig 1: SR Flipflop**

**SR Flipflop truth table**

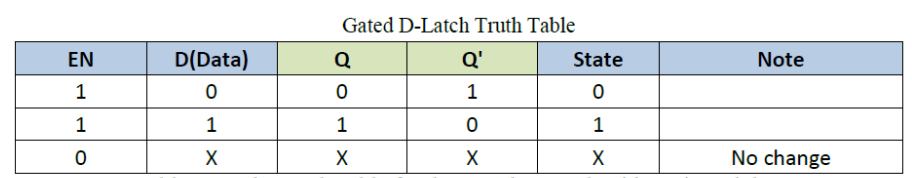


The gated D latch (D for data) can be built by adding an inverter before each of the two inputs in a gated S-R latch. A gated D latch is also called a level-triggered D flip-flop (D FF). Its diagram is shown in Figure 2.



**Fig 2: Gated D-latch with active high EN.**

A level-triggered D FF has a simple operation. The output Q simply follows the data input D when the enable input is activated. Q is latched when the enable is low. There is no invalid state in this latch.



### **VHDL Code for SR Flipflop**

|  |
| --- |
| **library** ieee; |

|  |
| --- |
| **use** ieee. std\_logic\_1164.**all**; |

|  |
| --- |
| **use** ieee. std\_logic\_arith.**all**; |

|  |
| --- |
| **use** ieee. std\_logic\_unsigned.**all**; |

|  |
| --- |
|  |

|  |
| --- |
| **entity** SR\_FF **is** |

|  |
| --- |
| **PORT**( S,R,CLOCK: **in** std\_logic; |

|  |
| --- |
| Q, QBAR: **out** std\_logic); |

|  |
| --- |
| **end** SR\_FF; |

|  |
| --- |
|  |

|  |
| --- |
| Architecture behavioral **of** SR\_FF **is** |

|  |
| --- |
| **begin** |

|  |
| --- |
| **PROCESS**(CLOCK) |

|  |
| --- |
| **variable** tmp: std\_logic; |

|  |
| --- |
| **begin** |

|  |
| --- |
| **if**(CLOCK='1' **and** CLOCK'EVENT) **then** |

|  |
| --- |
| **if**(S='0' **and** R='0')**then** |

|  |
| --- |
| tmp:=tmp; |

|  |
| --- |
| **elsif**(S='1' **and** R='1')**then** |

|  |
| --- |
| tmp:='Z'; |

|  |
| --- |
| **elsif**(S='0' **and** R='1')**then** |

|  |
| --- |
| tmp:='0'; |

|  |
| --- |
| **else** |

|  |
| --- |
| tmp:='1'; |

|  |
| --- |
| **end** **if**; |

|  |
| --- |
| **end** **if**; |

|  |
| --- |
| Q <= tmp; |

|  |
| --- |
| QBAR <= **not** tmp; |

|  |
| --- |
| **end** **PROCESS**; |

|  |
| --- |
| **end** behavioral; |

**VHDL Code for** **gated D\_latch with active high En:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity D\_latch is

generic (delay: time: =2 ns);

Port ( din : in STD\_LOGIC;

clock: in STD\_LOGIC;

q: out STD\_LOGIC;

q\_n:out STD\_LOGIC);

end D\_latch;

architecture D\_latch\_arch of D\_latch is

signal q\_temp: STD\_LOGIC;

begin

process (din, clock)

begin

if (clock = '1') then

q\_temp<=din after delay;

end if;

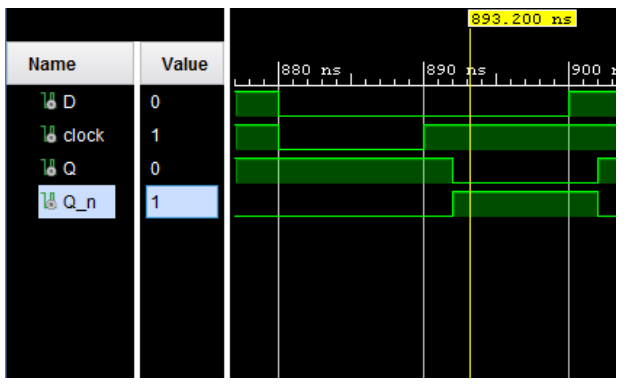
end process;

q<=q\_temp;

q\_n<=not q\_temp;

end D\_latch\_arch;

Output Waveform:



#### Pre-lab questions:

1. What is a flipflop and its types?
2. Give some flipflop applications
3. What is difference between latch and flipflop?
4. What is the difference between positive and negative edge triggering?

#### Post-lab questions:

1. How is D-flipflop obtained from a R-S flipflop?
2. Write a VHDL code for SR flipflop using dataflow modelling.

#### Result: